**CS530 Assignment 2 Report**

**Name:** Sri Krishna Chaitanya Velamakanni

**Email Id:** vzs5369@psu.edu

**Experiment Design**

In this study, I conducted a series of experiments to investigate the impact of cache size and associativity on cache performance, including area, energy consumption, and access time. The experiments were designed to provide insights into how different cache configurations affect these key performance metrics.

**Experiment 1: Area**

**a. Impact of Increasing Cache Size with Fixed Associativity (4):**

I analyzed the effect of increasing the cache size while maintaining a fixed associativity of 4. Cache sizes ranged from 16 KB to 2 MB. The goal was to understand how changes in cache size influence the physical area occupied by the data array.

**b. Impact of Increasing Associativity with Fixed Cache Size (128 KB):**

I investigated the impact of varying associativity while keeping the cache size fixed at 128 KB. Associativity values were tested from 1 to 32. The objective was to determine how different associativity levels affect the area of the data array.

**Experiment 2: Energy**

**a. Impact of Increasing Cache Size on Total Dynamic Read Energy per Access with Fixed Associativity (4):**

I measured the total dynamic read energy per access for the data array while varying the cache size. The associativity was held constant at 4. Cache sizes spanned from 16 KB to 2 MB. This experiment aimed to quantify the energy consumption under different cache size conditions.

**b. Impact of Increasing Associativity on Total Dynamic Read Energy per Access with Fixed Cache Size (128 KB):**

I explored the effect of changing associativity on the total dynamic read energy per access with a fixed cache size of 128 KB. Associativities were tested from 1 to 32. The goal was to understand how varying associativity influences energy efficiency.

**Experiment 3: Access Time**

**a. Impact on the Access Time with Varying Associativity and Fixed Cache Size (512 KB):**

I measured access times while varying the associativity of the cache and keeping the cache size constant at 512 KB. Associativity values ranged from 1 to 32. This experiment aimed to assess how different associativity levels affect access latency.

**b. Impact on the Access Time with Varying Cache Size (Range: 64 KB to 2 MB) and Fixed Associativity (4):**

I assessed access times while varying the cache size within the range of 64 KB to 2 MB, with a fixed associativity of 4. The objective was to understand how changes in cache size influence access latency.

These experiments were conducted to provide valuable insights into the trade-offs and optimizations available when configuring cache memory systems for specific applications and performance requirements. The results will contribute to the understanding and improvement of cache design in computer architecture.

**Experiment 1A (Cache Size Vs Area)**

The experiments clearly show an exponential increase in cache area as cache size grows, underlining the trade-off between performance improvements and the substantial chip space required for larger caches.

**Experiment 1B**

This graph is quite interesting. It shows that area and energy is unchanged for associativity 1 2 and 4. This shows that for low associativity when memory size is large, these factors don’t matter. As we scale up and keep memory constant, the area and energy increase, which shows that it is becomes the more dominant factor. This is because more circuits are needed to decode the tag and then hit the correct set. We add more comparators and complex multiplexers to achieve the goal of associativity. This causes an increase in area to realise the circuit and energy to drive it.

**Experiment 2A**

It is interesting to observe this trend because we intuitively think that increasing memory should decrease access time. But this is not the case due to physical constraints because the distance of the components increases to accommodate for a larger cache. The number of misses will decrease improving performance, but data access time increases as it must fetch from locations farther away due to its size.

**Experiment 2B**

This graph follows a similar trend as observed in Experiment 1B. Up to a given associativity for a certain cache size, the access time remains constant or very slightly increases. Beyond that, there is a lot of computation involved to decode the bits and hit the correct set, fetch the data. This is due to the additional comparators and multiplexer. This reduces the miss rates but increases access time.

**Conclusion**

We observe that increasing the cache size/associativity generally causes an increase in the energy, physical size and access time for a cache. However, these are not the only markers for cache performance, the number of hits, misses and AMAT should also be taken into consideration, along with the reduction in number of accesses required to the main memory, which increase the performance of the overall system.

**Code**

I have modified the code to reduce the logs in the output. The updated code along with cache configs (folder name: assignment\_config) and logs (Assignment 2 logs.ipynb) in the github url - [TanmayAmbadkar/cacti: An integrated cache and memory access time, cycle time, area, leakage, and dynamic power model (github.com)](https://github.com/TanmayAmbadkar/cacti)